



2824

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

<b>In re U.S. Patent Application</b>	)	
	)	
<b>YAMADA <i>et al.</i></b>	)	
	)	
<b>Application No. 09/982,839</b>	)	<b>Art unit: 2824</b>
	)	
<b>Filed: October 22, 2001</b>	)	<b>Examiner:</b>
	)	<b>LE, VU ANH</b>
<b>For: A SEMICONDUCTOR DEVICE, A METHOD OF</b>	)	
<b>MANUFACTURING THE SAME AND STORAGE</b>	)	
<b>MEDIA</b>	)	
	)	
<b>Attorney Docket No. HITA.0112</b>	)	

**Honorable Assistant Commissioner  
for Patents  
Washington, D.C. 20231**

**RESPONSE AND AMENDMENT UNDER 37 C.F.R. §1.111**

Sir:

This is in response to the Office Action dated April 5, 2004, the shortened period for response to which will expire on May 5, 2004. Applicants hereby elect the continuing prosecution of Group I, Species I, drawn to a layout of a memory device depicted in Fig. 1, without traverse. Claims 1-4, 6, 7, 13, 14, 17, 20-22, 30, 31, 33-37 and 39 pertain to the elected group.